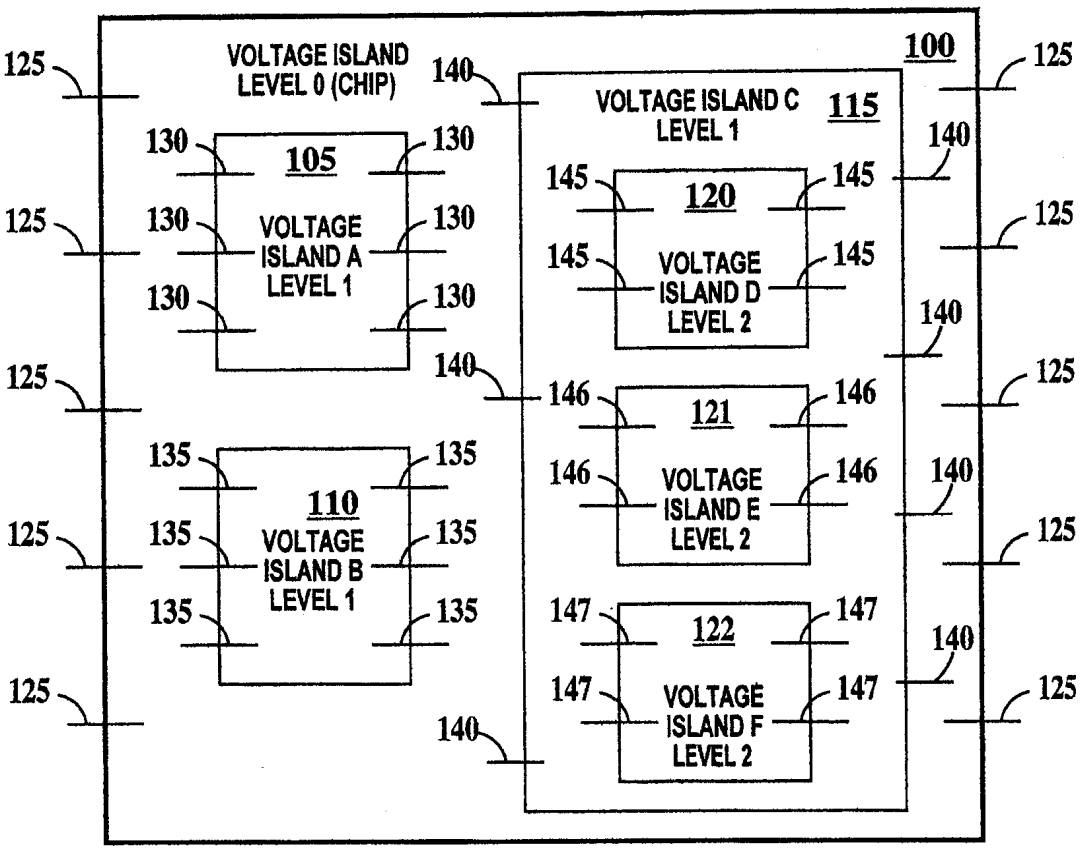
100
VOLTAGE ISLAND LEVEL 0 (CHIP)
105
VOLTAGE ISLAND A LEVEL 1
110
VOLTAGE ISLAND B LEVEL 1
VOLTAGE ISLAND C LEVEL 1
115
120
VOLTAGE ISLAND D LEVEL 2
121
VOLTAGE ISLAND E LEVEL 2
122
VOLTAGE ISLAND F LEVEL 2
125
130
135
140
145
146
147

FIG. 1

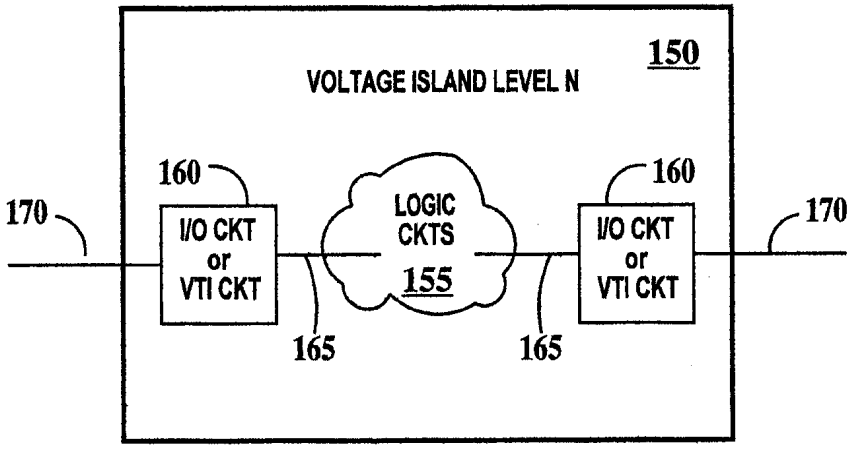
150
VOLTAGE ISLAND LEVEL N
160
I/O CKT or VTI CKT
LOGIC CKTS
155
165
170

FIG. 2

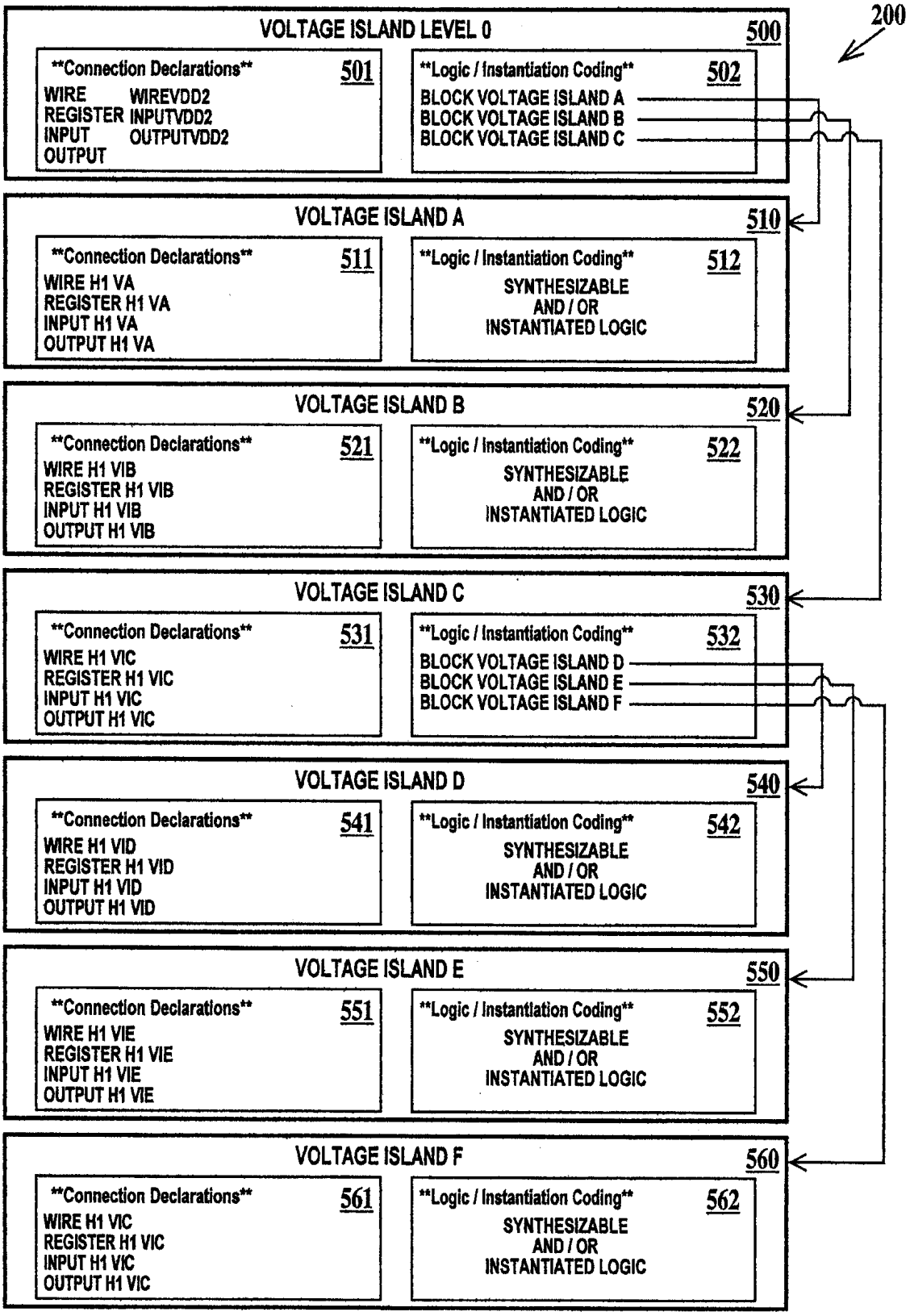
200
VOLTAGE ISLAND LEVEL 0
500
Connection Declarations
501
WIRE WIREVDD2
REGISTER INPUTVDD2
INPUT OUTPUTVDD2
OUTPUT
Logic / Instantiation Coding
502
BLOCK VOLTAGE ISLAND A
BLOCK VOLTAGE ISLAND B
BLOCK VOLTAGE ISLAND C
VOLTAGE ISLAND A
510
Connection Declarations
511
WIRE H1 VA
REGISTER H1 VA
INPUT H1 VA
OUTPUT H1 VA
Logic / Instantiation Coding
512
SYNTHESIZABLE
AND / OR
INSTANTIATED LOGIC
VOLTAGE ISLAND B
520
Connection Declarations
521
WIRE H1 VIB
REGISTER H1 VIB
INPUT H1 VIB
OUTPUT H1 VIB
Logic / Instantiation Coding
522
SYNTHESIZABLE
AND / OR
INSTANTIATED LOGIC
VOLTAGE ISLAND C
530
Connection Declarations
531
WIRE H1 VIC
REGISTER H1 VIC
INPUT H1 VIC
OUTPUT H1 VIC
Logic / Instantiation Coding
532
BLOCK VOLTAGE ISLAND D
BLOCK VOLTAGE ISLAND E
BLOCK VOLTAGE ISLAND F
VOLTAGE ISLAND D
540
Connection Declarations
541
WIRE H1 VID
REGISTER H1 VID
INPUT H1 VID
OUTPUT H1 VID
Logic / Instantiation Coding
542
SYNTHESIZABLE
AND / OR
INSTANTIATED LOGIC
VOLTAGE ISLAND E
550
Connection Declarations
551
WIRE H1 VIE
REGISTER H1 VIE
INPUT H1 VIE
OUTPUT H1 VIE
Logic / Instantiation Coding
552
SYNTHESIZABLE
AND / OR
INSTANTIATED LOGIC
VOLTAGE ISLAND F
560
Connection Declarations
561
WIRE H1 VIC
REGISTER H1 VIC
INPUT H1 VIC
OUTPUT H1 VIC
Logic / Instantiation Coding
562
SYNTHESIZABLE
AND / OR
INSTANTIATED LOGIC

FIG. 3

VOLTAGE DOMAIN DEFINITION FILE 205

CONNECTION DECLARATION	GLOBAL	VOLTAGE ISLAND	FLATTEN LEVEL	OFF CHIP SUPPLY	REGULATED SUPPLY	SUPPLY HEADER	CONTROLLED FROM	GND NOISE ISOLATED	VSS RAIL VALUE (V)	VDD RAIL VALUE (V)	EXTERNAL NOISE SUPPRESION REQURIED
WIRE	Y			Y					0.0	1.2	
REGISTER	Y			Y					0.0	1.2	
INPUT	Y			Y					0.0	1.2	
OUTPUT	Y			Y					0.0	1.2	
WIREVDD2	Y			Y					0.0	2.5	
INPUTVDD2	Y			Y					0.0	2.5	
OUTPUTVDD2	Y			Y					0.0	2.5	
WIRE H1 VIA		Y			Y		WIRE VDD2		-0.5	1.5	Y
REGISTER H1 VIA		Y			Y		WIRE VDD2		-0.5	1.5	Y
INPUT H1 VIA		Y			Y		WIRE VDD2		-0.5	1.5	Y
OUTPUT H1 VIA		Y			Y		WIRE VDD2		-0.5	1.5	Y
WIRE H1 VIB		Y				Y	WIRE		0.0	1.2	
REGISTER H1 VIB		Y				Y	WIRE		0.0	1.2	
INPUT H1 VIB		Y				Y	WIRE		0.0	1.2	
OUTPUT H1 VIB		Y				Y	WIRE		0.0	1.2	
WIRE H1 VIC		Y		Y					0.0	1.2	
REGISTER H1 VIC		Y		Y					0.0	1.2	
INPUT H1 VIC		Y		Y					0.0	1.2	
OUTPUT H1 VIC		Y		Y					0.0	1.2	
WIRE H1 VID		Y		Y				Y	0.0	1.75	Y
REGISTER H1 VID		Y		Y				Y	0.0	1.75	Y
INPUT H1 VID		Y		Y				Y	0.0	1.75	Y
OUTPUT H1 VID		Y		Y				Y	0.0	1.75	Y
WIRE H1 VIE		Y	WIRE H1 VC								
REGISTER H1 VIE		Y	REGISTER H1 VC								
INPUT H1 VIE		Y	INPUT H1 VC								
OUTPUT H1 VIE		Y	OUTPUT H1 VC								

FIG. 4

DESIGN CONSTRAINT FILE 210

CONNECTION DECLARATION	VDD NOISE TARGET (mV)	VSS NOISE TARGET (mV)	VDD DROOP TARGET (mV)	VSS DROOP TARGET (mV)	OPERATING FREQUENCY (MHz)	SWITCHING FACTOR %	CLOCK CYCLE OFFSET (%)
WIRE	300	200	100	100	80	50	0
REGISTER	300	200	100	100	80	50	0
INPUT	300	200	100	100	80	50	0
OUTPUT	300	200	100	100	80	50	0
WIREVDD2	400	300	200	200	40	50	50
INPUTVDD2	400	300	200	200	40	50	50
OUTPUTVDD2	400	300	200	200	40	50	50
WIRE H1 VIA	100	50	100	100	160	50	0
REGISTER H1 VIA	100	50	100	100	160	50	0
INPUT H1 VIA	100	50	100	100	160	50	0
OUTPUT H1 VIA	100	50	100	100	160	50	0
WIRE H1 VIB	100	100	200	200	20	30	50
REGISTER H1 VIB	100	100	200	200	20	30	50
INPUT H1 VIB	100	100	200	200	20	30	50
OUTPUT H1 VIB	100	100	200	200	20	30	50
WIRE H1 VIC	100	100	50	50	200	50	0
REGISTER H1 VIC	100	100	50	50	200	50	0
INPUT H1 VIC	100	100	50	50	200	50	0
OUTPUT H1 VIC	100	100	50	50	200	50	0
WIRE H1 VID	100	50	25	25	200	50	0
REGISTER H1 VID	100	50	25	25	200	50	0
INPUT H1 VID	100	50	25	25	200	50	0
OUTPUT H1 VID	100	50	25	25	200	50	0

FIG. 5

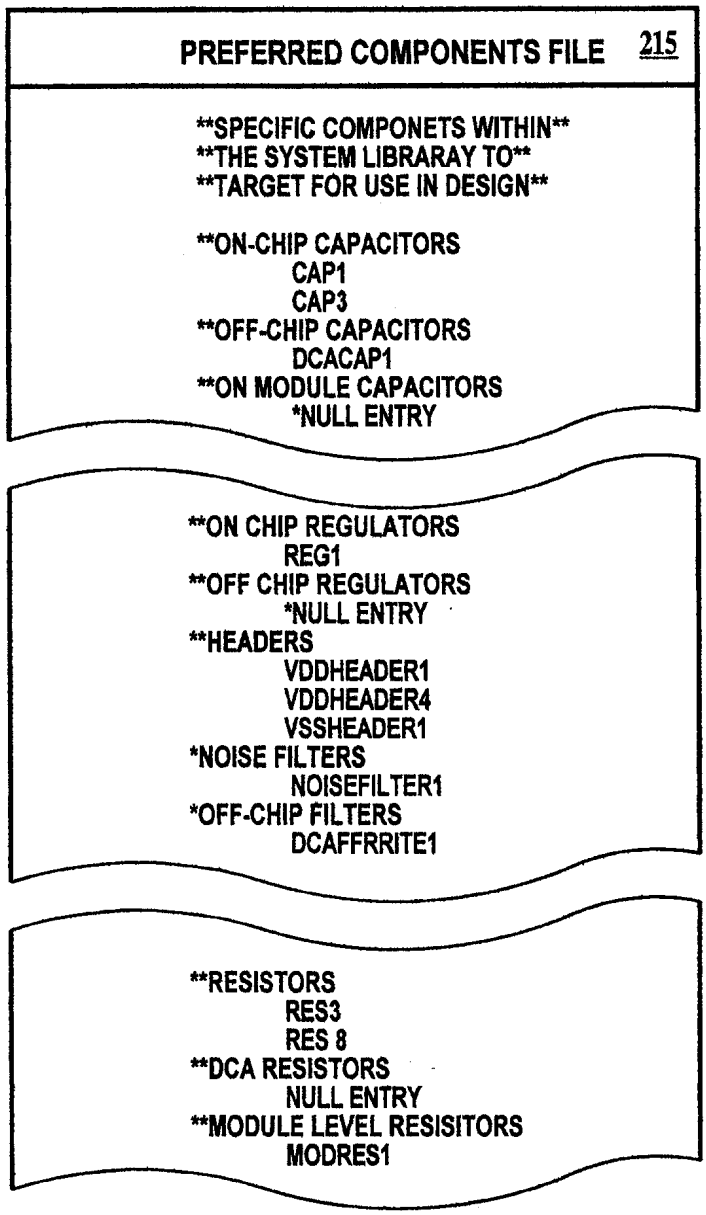
PREFERRED COMPONENTS FILE 215
SPECIFIC COMPONETS WITHIN
THE SYSTEM LIBRARAY TO
TARGET FOR USE IN DESIGN
**ON-CHIP CAPACITORS
CAP1
CAP3
**OFF-CHIP CAPACITORS
DCACAP1
**ON MODULE CAPACITORS
*NULL ENTRY
**ON CHIP REGULATORS
REG1
**OFF CHIP REGULATORS
*NULL ENTRY
**HEADERS
VDDHEADER1
VDDHEADER4
VSSHEADER1
*NOISE FILTERS
NOISEFILTER1
*OFF-CHIP FILTERS
DCAFFRRITE1
**RESISTORS
RES3
RES 8
**DCA RESISTORS
NULL ENTRY
**MODULE LEVEL RESISITORS
MODRES1

FIG. 6

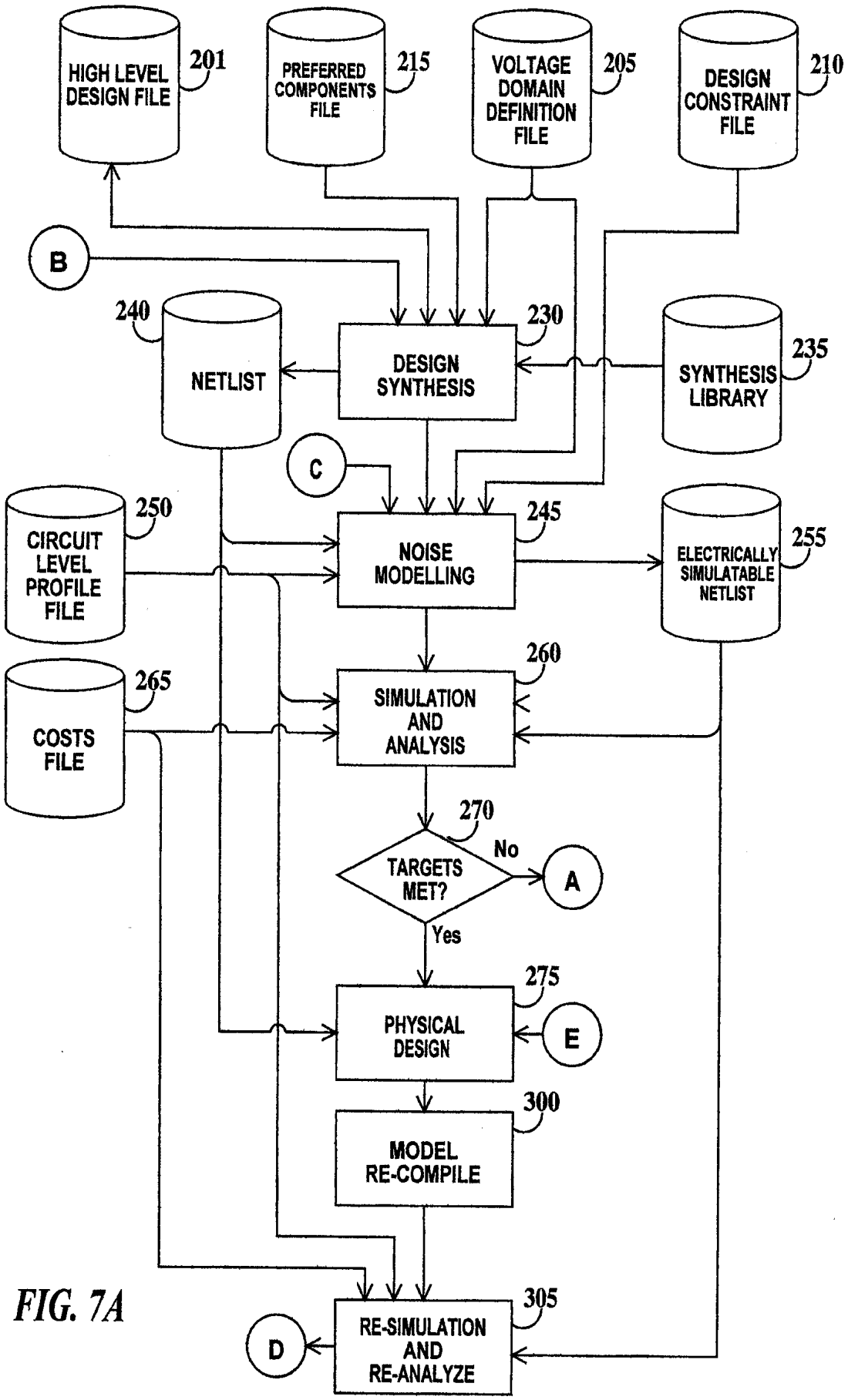
HIGH LEVEL DESIGN FILE
201
PREFERRED COMPONENTS FILE
215
VOLTAGE DOMAIN DEFINITION FILE
205
DESIGN CONSTRAINT FILE
210
B
240
NETLIST
DESIGN SYNTHESIS
230
SYNTHESIS LIBRARY
235
C
250
CIRCUIT LEVEL PROFILE FILE
245
NOISE MODELLING
ELECTRICALLY SIMULATABLE NETLIST
255
260
265
COSTS FILE
SIMULATION AND ANALYSIS
270
TARGETS MET?
No
A
Yes
275
PHYSICAL DESIGN
E
300
MODEL RE-COMPILE
305
D
RE-SIMULATION AND RE-ANALYZE

FIG. 7A

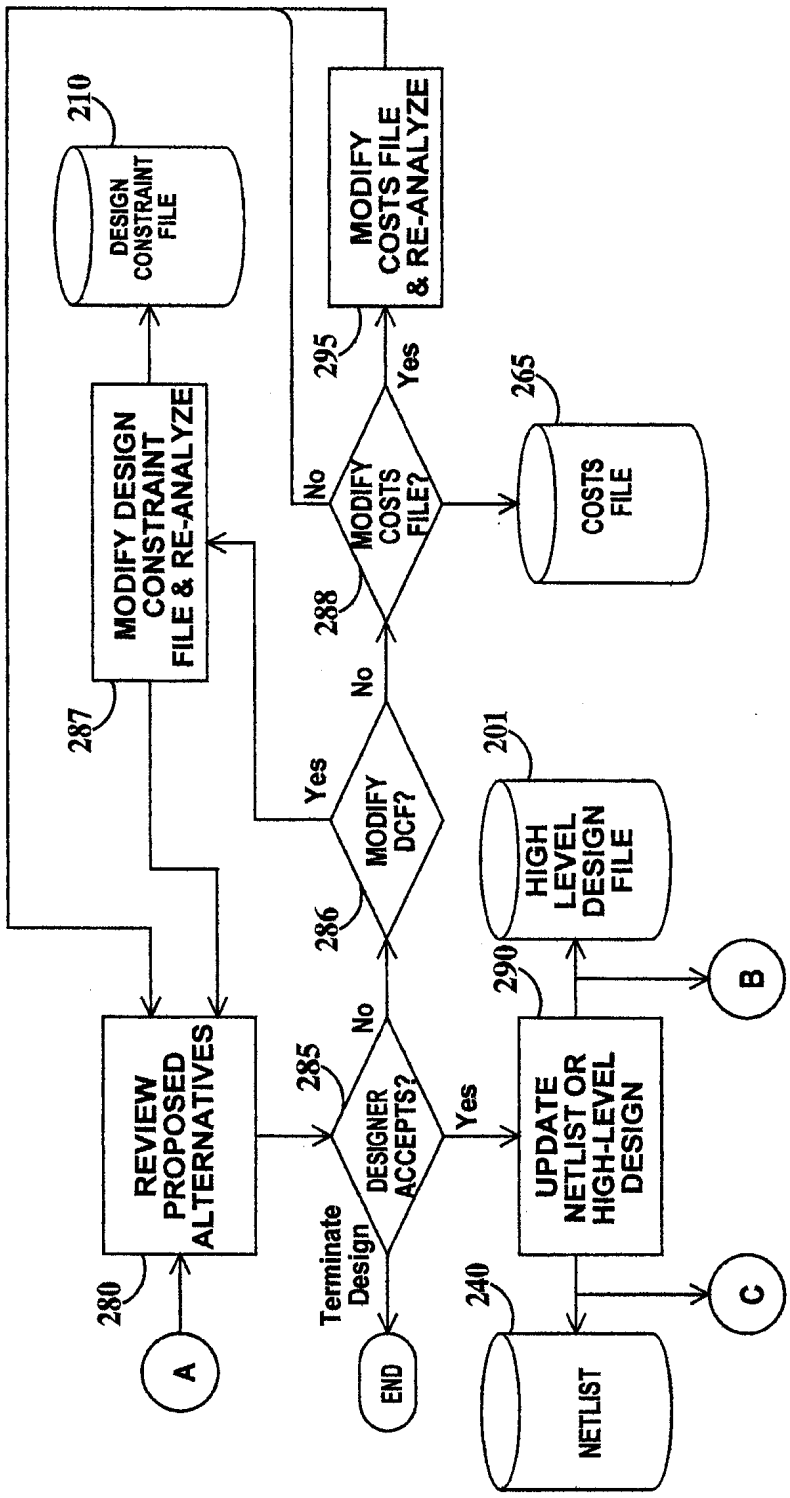
280
REVIEW PROPOSED ALTERNATIVES
285
DESIGNER ACCEPTS?
No
Yes
Terminate Design
END
286
MODIFY DCF?
No
Yes
287
MODIFY DESIGN CONSTRAINT FILE & RE-ANALYZE
210
DESIGN CONSTRAINT FILE
288
MODIFY COSTS FILE?
No
Yes
295
MODIFY COSTS FILE & RE-ANALYZE
265
COSTS FILE
290
UPDATE NETLIST OR HIGH-LEVEL DESIGN
201
HIGH LEVEL DESIGN FILE
240
NETLIST
A
B
C

FIG. 7B

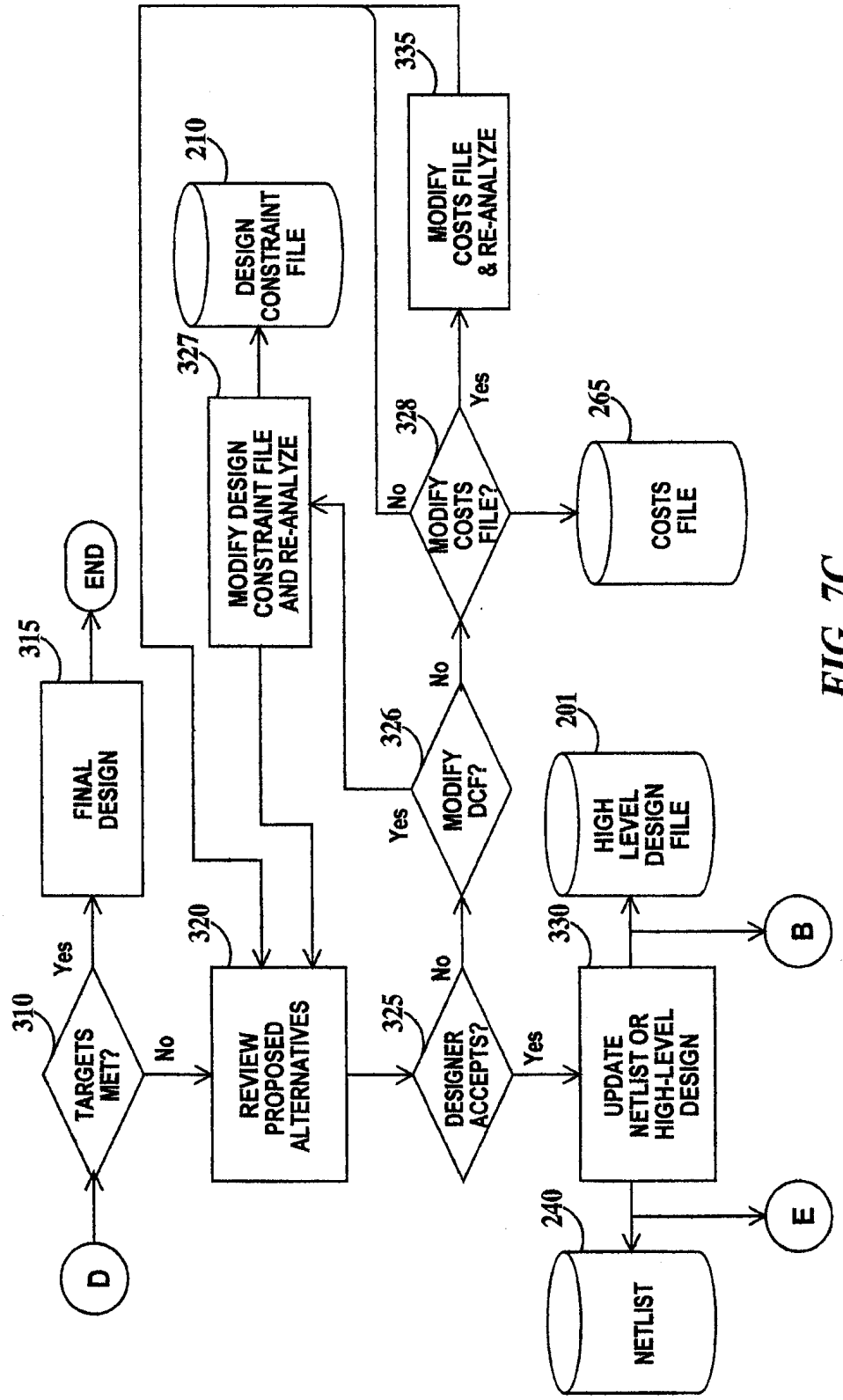
D
TARGETS MET?
310
Yes
No
FINAL DESIGN
315
END
REVIEW PROPOSED ALTERNATIVES
320
DESIGNER ACCEPTS?
325
No
Yes
MODIFY DCF?
326
Yes
No
MODIFY DESIGN CONSTRAINT FILE AND RE-ANALYZE
327
DESIGN CONSTRAINT FILE
210
MODIFY COSTS FILE?
328
No
Yes
MODIFY COSTS FILE & RE-ANALYZE
335
COSTS FILE
265
UPDATE NETLIST OR HIGH-LEVEL DESIGN
330
HIGH LEVEL DESIGN FILE
201
B
NETLIST
240
E

FIG. 7C

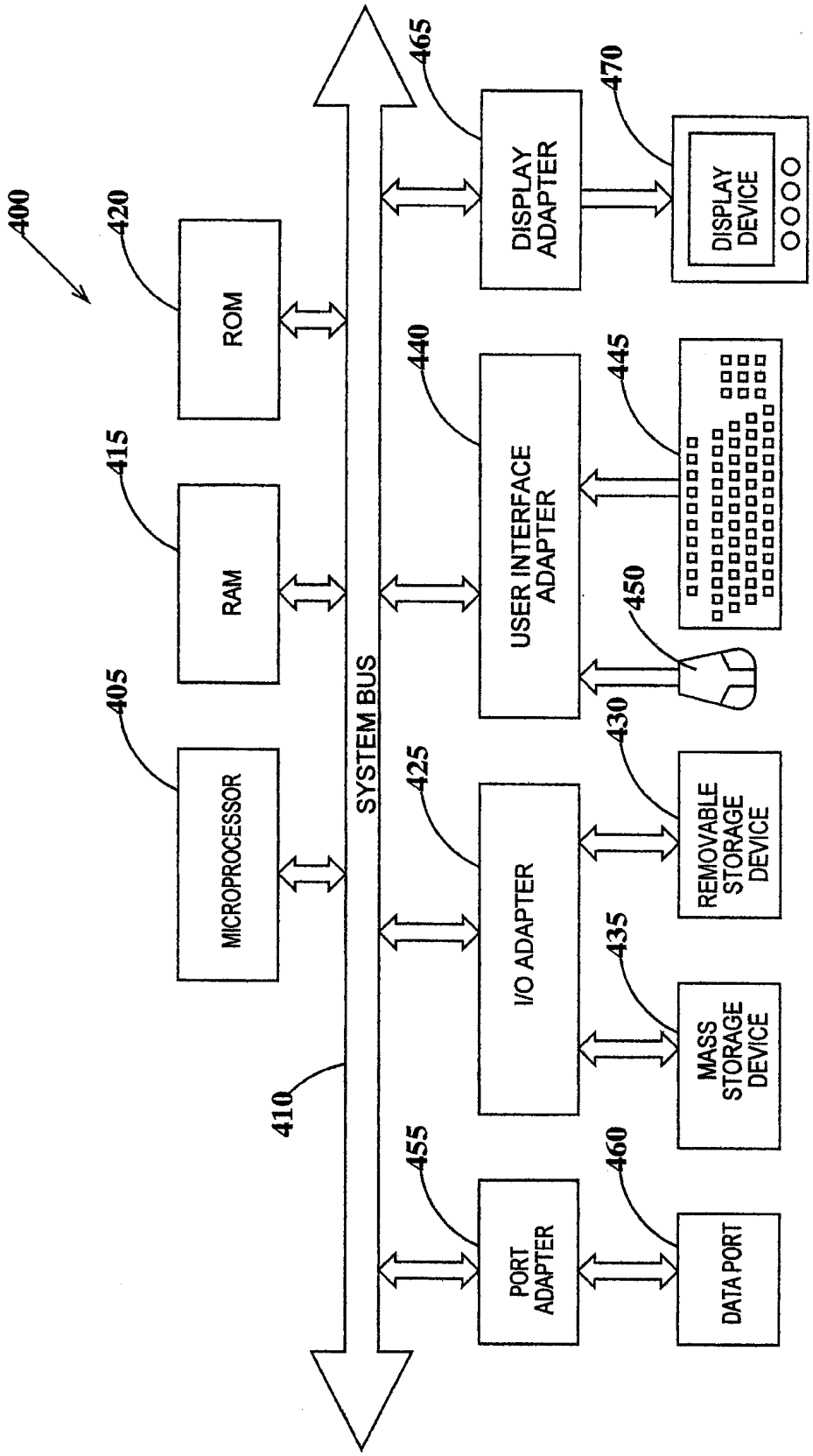
400
420
ROM
415
RAM
405
MICROPROCESSOR
SYSTEM BUS
410
465
DISPLAY ADAPTER
470
DISPLAY DEVICE
440
USER INTERFACE ADAPTER
445
450
425
I/O ADAPTER
430
REMOVABLE STORAGE DEVICE
435
MASS STORAGE DEVICE
455
PORT ADAPTER
460
DATA PORT

FIG. 8